AMENDMENT TRANSMITTAL LETTER (Large Entity) Applicant(s): Adkisson et al.						• •	BUR919	Docket No. 9990299 (01240161BA)	
Serial No. 10/064,171			Filing Date 06/18/2002		Examiner T. Magee			Group Art Unit 2811	
Invention: DOI	<u>~</u> /	ATE TRENCH	TRANSISTOR		•				
TO THE COMMISSIONER FOR PATENTS:									
Transmitted herev				• •	cation.				
. CLAIMS AS AMENDED									
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT		RATE	ADDITIONAL FEE	
TOTAL CLAIMS	8	•	20 =		0	х	\$18.00	\$0.00	
INDEP. CLAIMS			3 =		0	×	\$84.00	\$0.00	
Multiple Dependent Claims (check if applicable)								\$0.00	
TOTAL ADDITIONAL FEE FOR THIS AMEND HENT # \$0.00									
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Marshall M. Cur Reg. No. 33,138 Whitham, Curtis 11491 Sunset Hill Reston, VA 20190 (703) 787-9400	tis & Christ s Road, S		Cust	Dated	on first class ma Commission 22313-1450.	t this ail une er for	wil der 37 C.F.R Patents, P.C	and fee is being deposited th the U.S. Postal Service as . 1.8 and is addressed to the D. Box 1450, Alexandria, VA	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of James W. Adkisson et al.

Serial No.: 10/064,171√

Group Art Unit: 2811

Filed: June 18, 2002

Examiner: T. Magee

For: DOUBLE GATE TRENCH TRANSISTOR

Commissioner for Patents United States Patent and Trademark Office P. O. Box 1450 Alexandria, Virginia 22313-1450

AMENDMENT UNDER 37 C. F. R. §1.111

Sir:

In response to the Office Action mailed March 27, 2003, please amend the above-identified application as follows:

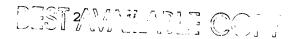
## In the specification:

Please replace paragraph 0021 with the following paragraph. A marked-up copy thereof showing currestly requested changes is provided in the Appendix to this response.

## Paragraph 0021:

The SOI wafer, as described above will generally include a thick so-called handling wafer or substrate 10 covered by a buried oxide (BOX) 12. Monocrystalline semiconductor layer 14, in turn, covers the buried oxide 12. Doping levels are relatively low in the preferred embodiment of this device, with the requirement that the channel be fully depleted. Typical doping levels are preferably in the 10<sup>15</sup>/cm³ to  $10^{17}$ /cm³ range with the high  $10^{16}$ /cm³ range being

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preferred. The process of the present invention begins by forming a layer of pad nitride of about 100 nm thickness and a pad oxide of about 3 - 10 nm thickness over the silicon and patterning the nitride using a patterned resist 18. The silicon height will determine device width and is preferably in the range of 50-200 nm. Many suitable resists and lithographic techniques for patterning them are familiar to those skilled in the art and specifics thereof are unimportant to the practice of the invention.

## In the claims:

Please substitute the following claim 1 for the like-numbered claim as originally filed. A marked up copy of this claim showing the current changes is attached as an appendix to this amendment.



1. (Amended) A field effect transistor comprising a conduction channel of sub-lithographic width, source and drain regions located at opposite ends of said conduction channel, said source and drain regions having silicide sidewalls on a surface thereof, and

polysilicon gate regions on opposing sides of said conduction channel and recessed from said source and drain regions, said polysilicon gate regions having silicide sidewalls formed thereon.

## REMARKS

Claims 1 - 8 remain active in this application. Claims 9-17 have previously been canceled. The specification has been reviewed and an editorial revision made where seen to be appropriate. Claim 1 has been amended to improve form. Support for the amendments of the claims is found throughout the application, particularly in Figures 4, 4A, 5 and 5A